

**LISTING OF THE CLAIMS**

The following listing of claims will replace all prior versions and listings of claims in the application.

1.     **(Original)**     A circuit for multiplexing a plurality of data signals into an output data stream comprising:

    a plurality of circuit elements, wherein a transition of each circuit element of said plurality of circuit elements is clocked by a first clock signal, wherein an output of each circuit element of said plurality of circuit elements comprises an individual data signal of said plurality of data signals and wherein said first clock signal is substantially in-phase with said transition; and

    a selector coupled to said plurality of circuit elements for sequentially selecting each of said individual data signals to generate said output data stream, wherein said selector is clocked to control said selecting by a second clock signal, wherein said second clock signal is out of phase with respect to said first clock signal by a fixed offset.

2.     **(Original)**     The circuit as recited in Claim 1 wherein said fixed offset comprises a quadrature offset.

3.     **(Original)**     The circuit as recited in Claim 1 wherein said fixed offset comprises a delay.

4.     **(Original)**     The circuit as recited in Claim 3 wherein said delay comprises a quadrature delay.

5.     **(Original)**     The circuit as recited in Claim 1 further comprising a clock generator coupled to said selector for generating said fixed offset.

6.     **(Original)**     The circuit as recited in Claim 5 wherein said clock generator comprises a coupled oscillator circuit.

7. **(Original)** The circuit as recited in Claim 5 wherein said clock generator comprises a divide-by-two circuit.

8. **(Original)** The circuit as recited in Claim 3 wherein said delay comprises a propagation delay.

9. **(Original)** The circuit as recited in Claim 8 further comprising a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay.

10. **(Original)** The circuit as recited in Claim 1 further comprising a compensator coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit element, wherein said second clock signal is transmitted to said selector through said compensator.

11. **(Original)** The circuit as recited in Claim 10 wherein said compensator retards said second clock signal to said selector by a compensating delay.

12. **(Original)** The circuit as recited in Claim 11 wherein said compensating delay corresponds to said clock-to-data delay.

13. **(Original)** The circuit as recited in Claim 1 wherein a part of said plurality of circuit elements comprises a flip-flop.

14. **(Original)** In a circuit comprising a plurality of circuit elements for providing a data signal with transitions in response to a clock signal and a selector coupled to said plurality of circuit elements for selecting said data signal for an output data stream, a method for multiplexing a plurality of said data signals into an output data stream comprising:

providing first and second clock signals, wherein said second clock signal is out-of-phase with respect to said first clock signal by a fixed offset;

clocking said circuit elements with said first clock signal to control said transitions of said data signal; and

clocking said selector with said second clock to sequentially select a plurality of said data signals for said output data stream.

15. **(Original)** The method as recited in Claim 14 wherein said fixed offset comprises a quadrature offset.

16. **(Original)** The method as recited in Claim 14 wherein said fixed offset comprises a delay.

17. **(Original)** The method as recited in Claim 16 wherein said delay comprises a quadrature delay.

18. **(Original)** The method as recited in Claim 16 wherein said delay is generated by a clock generator coupled to said selector.

19. **(Original)** The method as recited in Claim 18 wherein said clock generator comprises a coupled oscillator circuit.

20. **(Original)** The method as recited in Claim 18 wherein said clock generator comprises a divide-by-two circuit.

21. **(Original)** The method as recited in Claim 16 wherein said delay comprises a propagation delay.

22. **(Original)** The method as recited in Claim 21 further comprising a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay.

23. **(Original)** The method as recited in Claim 22 further comprising the step of delaying said second clock signal by a compensating delay.

24. **(Original)** The method as recited in Claim 23 wherein said compensating delay corresponds to a delay from said first clock signal to said transitions.

25. **(Original)** A system for multiplexing a plurality of data signals into an output data stream comprising:

a plurality of circuit elements, wherein a transition of each circuit element of said plurality of circuit elements is clocked by a first clock signal, wherein an output of each circuit element of said plurality of circuit elements comprises an individual data signal of said plurality of data signals and wherein said first clock signal is substantially in-phase with said transition;

a selector coupled to said plurality of circuit elements for sequentially selecting each of said individual data signals to generate said output data stream, wherein said selector is clocked to control said selecting by a second clock signal, wherein said second clock signal is out of phase with respect to said first clock signal by a fixed quadrature delay; and

a compensator coupled to said selector for compensating for a clock-to-data delay corresponding to said transition of each said circuit element, wherein said second clock signal is transmitted to said selector through said compensator, wherein said compensator retards said second clock signal to said selector by a compensating delay corresponding to said clock-to-data delay.

26. **(Original)** The system as recited in Claim 25 further comprising a clock generator coupled to said selector for generating said fixed quadrature delay.

27. **(Original)** The system as recited in Claim 26 wherein said clock generator comprises a circuit selected from the group consisting essentially of a coupled oscillator circuit and a divide-by-two circuit.

28.     **(Original)**     The system as recited in Claim 26 wherein said quadrature delay comprises a propagation delay.

29.     **(Original)**     The system as recited in Claim 28 wherein said clock generator comprises a section of a transmission medium coupled to said selector wherein said section comprises a particular length, wherein said particular length corresponds to said propagation delay.

30.     **(Original)**     The system as recited in Claim 25 wherein a part of said plurality of circuit elements comprises a flip-flop.